Obtaining Constant Transconductance in Multimodal Thin-Film Transistors Towards High-Yield Roll-to-Roll Manufacturing

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ABSTRACT

Large area electronic circuit design would benefit from highly functional, yet compact, circuits that take advantage of an extremely linear dependence of output current on input voltage, such as digital-to-analog converters, linear voltage-to-current converters and low distortion amplifiers. Here, we show that constant transconductance in a multimodal transistor can offer directly proportional dependence with source geometries suitable for roll-to-roll manufacturing (> 10 µm).

Keywords: Thin-film transistor, Schottky barrier, uniformity, linearity.

1. INTRODUCTION

There are many promising future Internet of Things (IoT) and flexible electronics applications beyond display technology [1], some potentially lucrative if produced in low-cost, high-throughput manufacturing methods [2], [3]. Roll-to-roll (R2R) processes offer the most attractive route, but persistent device non-idealities associated with Ohmic contact thin-film transistors (TFTs) [4] have restricted progress, due to poor uniformity [5].

Breakthroughs are mainly process related, with little progress in TFT architectures. Indeed, back gates allow control of the threshold voltage, V_{th} [6], but these require external biasing, tailored to individual devices. Moreover, circuits comprising Ohmic contact TFTs typically require additional cascode or gain stages to improve performance. As the probability of circuit failure increases with the number of components [4], yield is further reduced. Thus, robust devices and compact circuits are particularly needed.

The multimodal transistor (MMT) [7] is a promising candidate for R2R manufacturing. This staggered-electrode architecture operates by separately controlling charge injection from channel conduction, using two control gates (Fig. 1a,b). As the MMT's charge injection principles are based on source-gated transistor (SGT) operation [8], [9], it shares many benefits [10] including: low saturation voltage; high gain; power efficiency; robustness to bias stress; and, notably, tolerance to electrode misalignments [11]. In addition, the MMT overcomes some of the SGT limitations and can provide a linear drain current dependence on input voltage in saturation (Fig. 1c,d) [7]. This allows for extremely compact, yet highly functional, circuits, such as a single-device multiplying digital-to-analog converter [12].

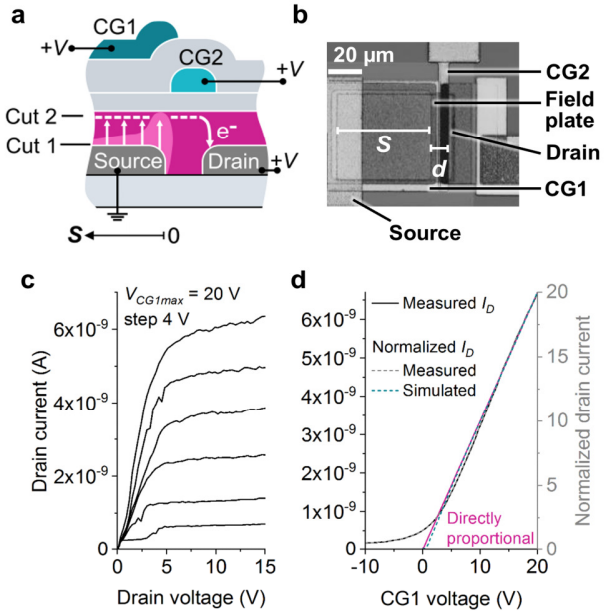

Figure 1: a) Cross-section of a multimodal transistor (MMT) with current control gate (CG1) and switching gate (CG2) from [7]. Source-CG1 overlap S is shown. As the source comprises an energy barrier, the switching gate in the channel does not modulate drain current. b) SEM of a µ-Si MMT. c) Output curves of a MMT (S = 54 µm) with low voltage saturation and constant transconductance g_m. d) A directly proportional dependence can be achieved in the MMT.

Linear circuit operations normally require operational amplifiers, which are complex in design. Ideally, circuits should be designed to perform a function with the minimal amount of components [13]. Hence, exploiting the MMT's linear behavior could lead to improvements in yield.

While the origins of constant transconductance g_m and the role of layer thickness have been explored in the MMT (including low-distortion amplification) [7], consideration needs to be given for obtaining this behavior in light of R2R fabrication, where feature sizes are generally large (> 10 µm) [2].

2. EXPERIMENTAL METHODS

2.1 Multimodal Transistor Fabrication

Preliminary MMTs were prototyped in microcrystalline silicon (μ-Si) using the Corial 210D reactor. The process begun with Al and SiO_2 deposition, starting with the current control gate (CG1), and was repeated for the switching gate (CG2). After the second SiO_2 layer, μ-Si was deposited via ICP-CVD [7] (2h 180 °C N_2 anneal), followed by 20 nm field plate SiO_2, which was etched to open contact windows. Ni was deposited for Schottky contacts. All steps were performed at 180 °C or lower. See [7] for full details.

2.2 Device Simulation

MMT simulations in default amorphous silicon (a-Si) parameters were performed using Silvaco Atlas TCAD suite. As charge injection is modulated by the source contact, the following parameters were considered: source-CG1 overlap S = 1, 4, 16 μm; and barrier height Φ_B = 0.45, 0.50, 0.55 eV. The semiconductor and gate insulator thickness were $t_s = t_i$ = 40 nm. As the channel does not modulate charge injection, the source-drain separation d was kept at 4 μm. The control gates, CG1 and CG2, were separated by a 1 μm gap, and an overhang was included on CG1 to provide a continuous electric field in the accumulation region (see Supplementary Material of [7] for material parameters). Simulated devices are not intended to represent a structure optimized for R2R processes, but allow observation of injection processes in the source region for a variety of sizes, shedding light on future device design.

3. RESULTS AND DISCUSSION

As the MMT is a contact-controlled device, the current control gate (CG1) provides charge injection based on a reverse biased energy barrier, in a manner similar to SGTs, where pinch-off occurs at the source edge [7], [9]. When drain potential reverse biases the source barrier, the semiconductor under the source edge forms a depletion region that extends across the entire width of the active layer. The capacitances per unit area of the insulator and semiconductor, C_i and C_s, respectively, determine the saturation voltage V_{DSAT} at the point of pinch-off. Hence, $V_{DSAT} = (V_{CG1} - V_{th1})(\ C_i\ /\ (C_i + C_s)) + K$, where K is a constant associated with the drain voltage required to deplete charge carriers at the insulator interface [9]. The output characteristics in Fig. 1c highlight the low V_{DSAT} of these devices, which can be tailored by altering the properties/geometry of C_i and C_s.

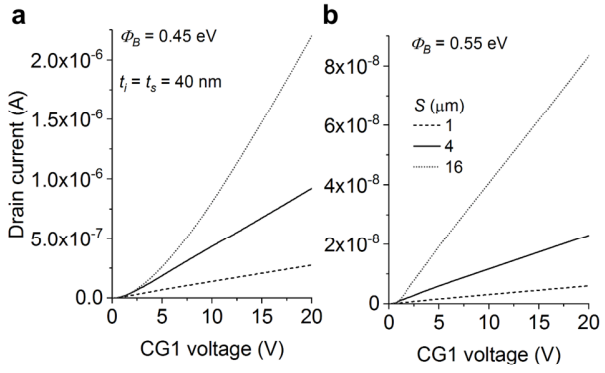

Figure 2: CG1 transfer characteristics with a) low and b) high source energy barriers. As MMTs are contact-, rather than channel, controlled, longer S allows for increased charge injection. Nonlinear dependence is observed for low barriers with longest S.

However, extremely low V_{DSAT} [10] and high gain can be traded-off to produce constant g_m [7] (Fig. 1d). As the channel plays no role in modulating drain current in the MMT, it simply acts as an on/off switch (controlled by CG2), providing a conductive path for drain current from the source region to flow (see [7] for CG2 transfer characteristics).

As the contact is responsible for charge injection, the design of the source region becomes important. While low barriers produce increased drain currents (Fig. 2), the saturation behavior improves for higher barriers [9]. The source-CG1 overlap S is also an important parameter, as g_m increases with S. Yet, this increase is not indefinite, as eventually the charge injected from the furthest region encounters too great a resistance in the accumulated layer at the insulator interface. Thus, drain current saturates at a value where increasing S no longer facilitates additional injection [9]. This is an advantageous feature, as current uniformity is ensured, irrespective of electrode misalignments.

In considering directly proportional dependence of output on input, the normalized g_m (Fig. 3) allows for visual comparison of behavior across different geometries. Where low barriers are concerned, only very short S can provide the necessary behavior, which is not easily achievable in R2R processes. [3]. However, higher source barriers promote direct proportionality in designs with a R2R-compatible range (Fig. 3c, S = 16 μm).

Additional insight is gained though cutlines of lateral current density $J_{e\text{-}Y}$ (taken 1 nm from the source interface)

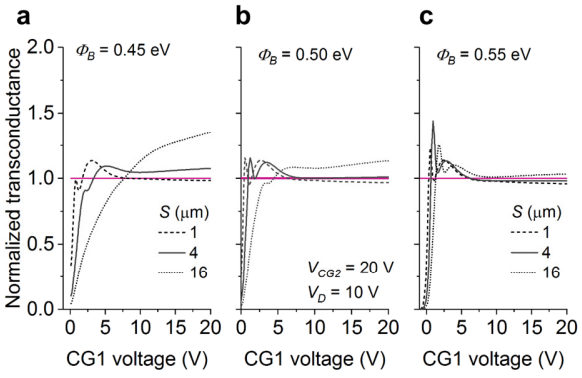

Figure 3: Normalized transconductance, allowing for comparisons between devices with barrier height a) Φ_B = 0.45 eV, b) Φ_B = 0.50 eV, and c) Φ_B = 0.55 eV. The fuchsia reference line indicates a directly proportional dependence. For low barriers, direct proportionality is achieved for short values of S, while a wider range of S achieves this in higher barriers.

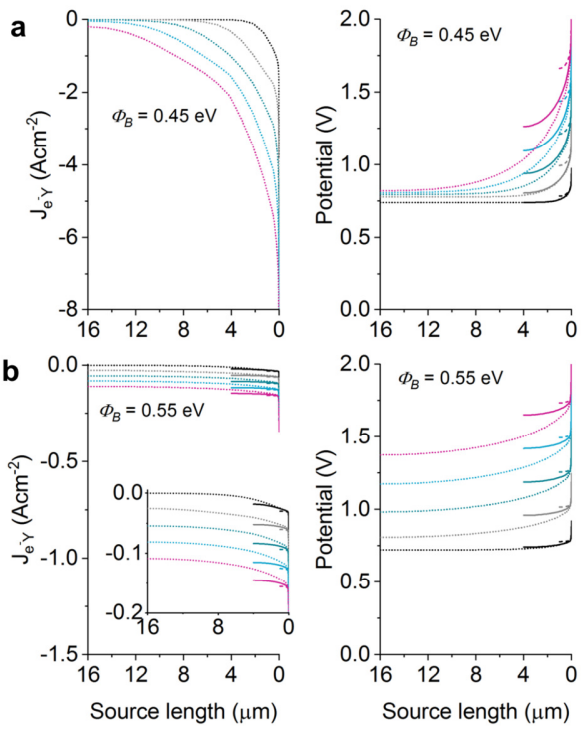

Figure 4: Lateral electron current density J_{e^-Y} from cutlines taken 1 nm along the source-semiconductor interface and potential in the accumulation layer 1 nm from the insulator interface for a) Φ_B = 0.45 eV, and b) Φ_B = 0.55 eV with close-up of J_{e^-Y} inset.

and potential (taken 1 nm from the insulator interface).

For long values of *S*, charge injection in the presence of the low electric field dominates over any thermionic-field emission at the source edge [8]. Injection thus involves the network of resistances vertically across the semiconductor and horizontally in the accumulation layer at the insulator interface. At each point along the distance of *S*, the resistance charge carriers encounter, along with the proportion of current determined by $V_{DSAT,}$ affects the nature of drain current [7]. Low barriers lead to higher current densities (Fig. 4a), which produce a high *IR* voltage drop in the accumulation layer. As such, in the furthest region of *S*, there is insufficient vertical potential difference to facilitate injection. In this case, only very short *S* can produce direct proportionality. For high barriers (Fig. 4b), the lower current leads to lower *IR* voltage drop. Hence, longer values of *S* can contribute to the injection process, where direct proportionality is observed when the traces of Fig. 4 are parallel and equally spaced.

When including other geometrical and material parameters, which also affect the linear behavior [7], device designers are equipped with various avenues for tuning MMTs to produce excellent linear behavior. In challenging manufacturing processes associated with R2R, larger overlaps would be favorable in these devices, which are readily and reliably achieved. While large overlaps and low g_m restrict operating speeds, numerous applications, e.g. biosensing, operate with signal bandwidths < 10 kHz, making the solution pertinent to a wide range of scenarios [7].

4. CONCLUSION

Aside from layer thicknesses and permittivities, constant transconductance with directly proportional dependence can be achieved through using higher source barriers to ensure the whole of the source-CG1 overlap contributes to injection. This has high potential for R2R fabricated circuits, where longer overlaps conveniently match what is generally considered an R2R limitation, thus using the area efficiently.

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