Low-Dimensional Heterojunction-Based Ternary Inverters Enabled by Inkjet Printing

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ABSTRACT

Multi-valued logic (MVL) circuits have been demonstrated by employing devices which exhibit negative differential resistance (NDR) or negative transconductance (NTC) characteristics, recently. In particular, anti-ambipolar transistors with NTC characteristics, where current increases to the peak current value and decreases after the peak value with an increase of gate voltages, have been implemented by forming van der Waals (vdW) heterojunction channels. However, most of the heterojunctions have been formed by non-scalable methods such as a mechanical exfoliation and a manual transferring. Herein, we present ternary inverter circuits whose channels are formed by fully scalable methods. vdW heterojunctions are formed by inkjet printing of p-type single-walled carbon nanotubes (SWCNTs) that partially overlap chemical vapor deposited (CVD) n-type MoS_2. Resultant anti-ambipolar transistors based on p-n heterojunctions exhibit NTC characteristics. Ternary inverter shows distinct three logic states at low operating voltages.

Keywords: inkjet printing; vdW heterojunction; ternary circuit; anti-ambipolar transistor; negative trans-conductance

1. INTRODUCTION

Multi-valued logic (MVL) circuits have been considered to be a promising candidate to overcome the limitation of the conventional binary logic circuits by expressing more than two logic states using a single logic gate.[1] Higher bit densities can be achieved by employing such MVL circuits, therefore the same operation can be performed with much less number of devices and interconnects compared to the case of binary circuits.[2] Recently, such MVL circuits have been demonstrated by employing van der Waals heterojunction-based devices with transconductance (NTC) characteristics. Heterojunction-based NTC devices, whose transfer characteristics show inverted V-shaped curves, are also called anti-ambipolar transistors since their transfer characteristics are opposite to those of ambipolar transistors.[3,4] Various two-dimensional (2D) semiconductors such as molybdenum disulfide (MoS_2) have been employed for implementation of heterojunction-based anti-ambipolar transistors because high-quality p-n heterojunctions can be easily formed with dangling bond-free 2D crystals. However, most of 2D semiconductor-based anti-ambipolar transistors have been fabricated by the mechanical exfoliation method, which is not suitable for actual applications due to its poor scalability.

In this work, we demonstrate ternary inverter circuits whose channels are formed by fully scalable methods. vdW p-n heterojunctions for anti-ambipolar transistors are formed by employing n-type MoS_2 monolayer grown by chemical vapor deposition (CVD) and inkjet printed p-type single-walled carbon nanotubes (SWCNTs). The heterojunction-based anti-ambipolar transistor shows NTC behavior. Moreover, a ternary inverter composed of the anti-ambipolar transistor and a SWCNT p-channel transistor shows a distinct middle-logic level in its voltage transfer characteristics (VTC).

2. METHODS

Figure 1 shows a schematic of the ternary inverter consists of a heterojunction-based anti-ambipolar transistor and a SWCNT p-type transistor. A MoS_2 monolayer was synthesized on another SiO_2/Si substrate by CVD, then transferred onto a HfO_2/Si substrate,[5] where HfO_2 was deposited by atomic layer deposition (ALD) as a gate dielectric for both transistors. Ag ink was inkjet printed (DMP-2850, Fujifilm) to form source/drain electrodes for n- and p-type transistors as well as anti-ambipolar transistors, followed by annealing at 150 °C for 15 min on a hotplate. After Ag annealing, the surface was treated with UV/O_3 (PSDP-UV4, Novascan) for 10 s to improve the wetting of SWCNT ink. The SWCNTs ink was prepared by dispersing SWCNTs (semiconducting purity > 98%, Nanointegris) in 1-cyclohexyl-2pyrrolidone (Sigma-Aldrich) at a concentration of 0.1 mg/mL. The channel of anti-ambipolar transistors were fabricated by forming p-n heterojunctions where random networks of inkjet printed SWCNTs were partially overlapped the MoS_2 monolayer. The SWCNT ink was printed to form the channel of the p-type transistor that was connected with the anti-ambipolar transistor as well. Then, the substrate was placed on a hotplate at 200°C for 30 min to remove residual solvents. All transistors and ternary inverter characteristics were measured using a semiconductor parameter analyzer (Agilent 4155C) under ambient conditions.

3. RESULTS

Before measuring ternary inverter characteristics, individual characteristics of n-, p-type and anti-ambipolar transistors were measured. In order to monitor characteristics of the n-type transistor, another MoS_2 transistor, whose channel is separated from the flake used for the heterojunction-based transistor, was fabricated and measured independently. Figure 2(a) and (b) shows transfer characteristic (I_D-V_{GS}) of the n- and p-type transistors, respectively. The n-type MoS_2 transistor ($W \sim 20$ μm, $L \sim 16$ μm) exhibits I_{on}/I_{off} of 1.19×10^5 and threshold voltage (V_{th}) of 0.78 V at $V_{DS} = 0.1$ V. The p-type SWCNT transistor ($W \sim 73$ μm, $L \sim 16$ μm) exhibits I_{on}/I_{off} of 4.54×10^4 and V_{th} of -0.11 V at $V_{DS} = -0.1$ V.

Figure 2(c) shows transfer characteristics of the anti-ambipolar transistor where I_D increases until it reaches to its maximum point (I_{max}), then I_D decreases as V_{GS} increases. The negative transconductance ($g_m = dI_D/dV_{GS}$), which is a unique characteristic of anti-ambipolar transistors, regions are shaded in red as shown in Figure 2(d).

The ternary inverter was constructed by connecting the anti-ambipolar transistor (as a pull-down transistor) with a p-type SWCNT transistor (as a pull-up transistor) as shown in Figure 3(a). Figure 3(b) shows VTC of the ternary inverter at $V_{DD} = 2$ V. Three distinct logic states are clearly observed in Figure 3(b). The middle logic state are displayed when channel resistances of both transistors become comparable. This occurs in the range of NTC where both anti-ambipolar and SWCNT transistor currents decrease as V_{GS} increases.

4. CONCLUSION

The ternary inverter was demonstrated by employing the anti-ambipolar transistor with the SWCNT transistor. The channel of the anti-ambipolar transistor was composed of heterojunctions of CVD grown MoS_2 and inkjet printed SWCNTs. Both CVD and inkjet printing methods are suitable for implementation of integrated circuits due to their scalability. In particular, inkjet printing allowed random networks of SWCNTs to be formed on a part of the MoS_2 flake in a controlled manner. The resultant heterojunction-based transistor showed NTC characteristics. Three distinct logic states were clearly presented in VTC by connecting the anti-ambipolar pull-down transistor with the p-type pull-up transistor.

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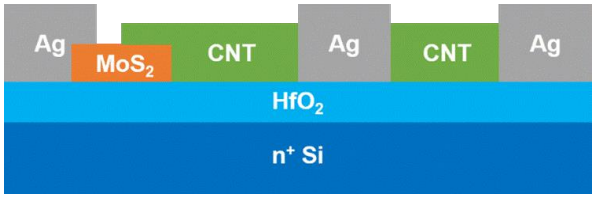

Figure 1: Schematic cross-section of the ternary inverter composed of a MoS_2/SWCNTs heterojunction-based anti-ambipolar transistor and a SWCNT p-type transistor.

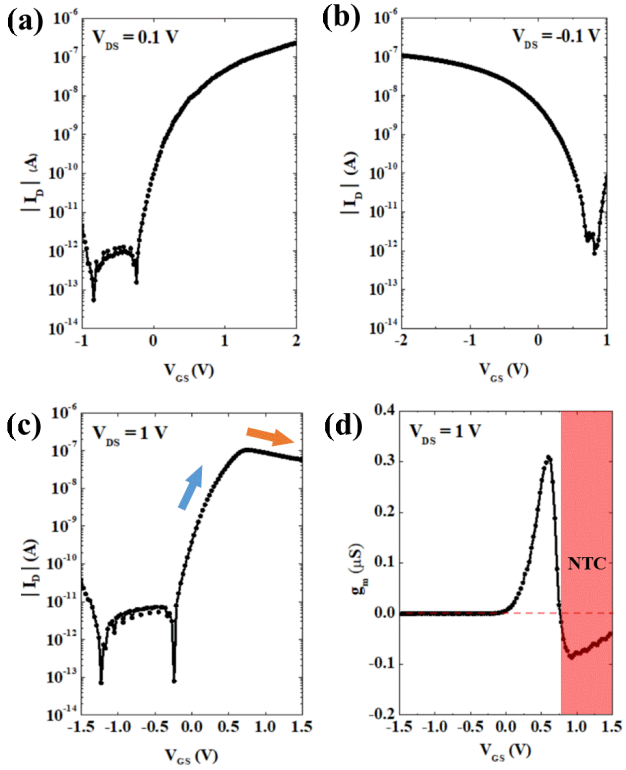

Figure 2: I_D-V_{GS} characteristics of (a) n-type MoS_2 transistor, (b) p-type SWCNT transistor, and (c) anti-ambipolar transistor. (d) Transconductance ($g_m = dI_D/dV_{GS}$) of the anti-ambipolar transistor as a function of V_{GS}.

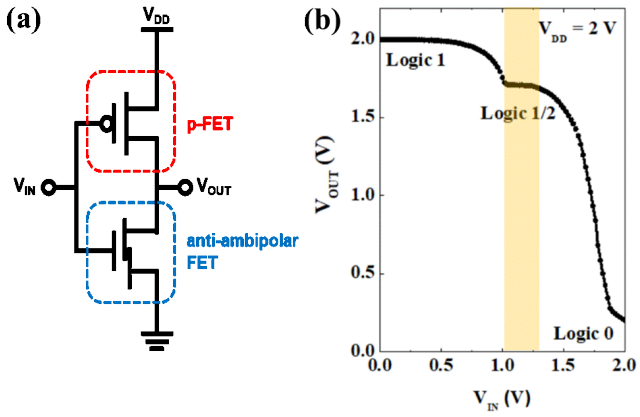

Figure 3: (a) Circuit configuration and (b) voltage transfer characteristics of the ternary inverter.